High-Performance ICs in Single-Supply Analog Circuits—Design Issues and Application Examples

by Walt Jung and James Wong

As system designers increasingly use single-supply power for both analog and digital circuits, they face challenges if they must obtain the kind of performance they are used to at higher voltages—and increased challenges if they seek to better it. This article examines some typical precision analog functions with op amps and other devices, using chips and application techniques designed to produce maximum benefit on single low-voltage (3-5-volt) supplies at low power. We first consider device limitations, then discuss examples of application circuits.

DESIGN ISSUES

Selecting Amplifiers

The choice of amplifier (or other analog chip) is a critical step toward a successful single-supply design. A source of helpful information, Table 1 lists typical specs of currently available Analog Devices op amps suitable for use on single supplies ≥3 V, in order of increasing power consumption per channel. Although most of these devices work over much wider voltage ranges, as well as on dual supplies, our emphasis is on their low-voltage single-supply behavior. Characteristics listed include single-supply voltage range and input- and output (grounded-load) common-mode ranges, for supply voltages ≤5 V. As the table indicates, many of the amplifiers are available as singles, duals, and even quads; and most come in both DIP and SOIC packages. Also listed are (5-V) quiescent currents per amplifier channel, output drive current, and basic dc & ac specifications. The following detailed discussions will provide further insight into specific amplifier design features.

Reduced Signal Range

Most op amps in use today are designed for traditional ±15-V supplies, which allows ample input common-mode (CM) voltage range, as well as a wide output range—typically ±10 V for both. Because power conservation is a major reason for using them, single-supply systems often have closely restricted supply voltage, for example, +12 V down to + 5 V, as low as +3 V, and even in some cases +1.5 V. At these low voltages most standard dual-supply op amps cease to function at all, while some may still operate with degraded specifications. Until recently, low-voltage amplifier choices have been limited.

General purpose 741s & 1558s, and most FET-input amplifiers operate on supplies as low as ±5 V (10 V total). Precision amplifier families such as OP-07 or OP-27 types don't work below ±5 V. Types from some selected families may be used over regions of this voltage spectrum; for example the AD705 & OP-97 families are useful down to ±2.25 V (4.5 V), and the AD817 wideband op amp is spec'd for +5-V use. But in general, only amplifiers that are specifically designed for single-supply use will function without major limits in CM range and output swing below +10 V. Examples are the LM324/LM358 families as general-purpose modest-performance single-supply types, and the devices of Table 1 for precision uses.

Watch Out for Input/Output Swing Limitations

Amplifiers designed for ±15-V operation typically need 2 to 5 V of headroom at input and output, with respect to both supply rails. Even more-flexible dual-supply designs, such as the AD705 & OP-97 families, approach only to within 1 V.

In low-voltage (3- to 5-V) single-supply applications, such headroom requirements become critical limitations to linear operation over even modest signal swings. For this reason, single-supply amplifier input stages are designed to remain fully linear, even when the input CM voltage is at the negative rail, or 0 V. Differential input-stage architectures allowing this involve PNP bipolars, CMOS (or PMOS) inputs, and N-channel JFET inputs. The various devices result in differing input bias currents, noise voltages/currents, and offset voltages/drifts. All the devices listed in Table 1 can operate with $V_{IN} = 0\ V$; at the upper end of the CM range, some devices can go to within 1 V of the rail, while others may need 1.5 V.

Table 1. Op-Amp Chips Compatible with 3- and 5-Volt Single-Supply Systems

Device/s	Amplifier[1] Channels	Supply[2] Range (V)	V_{IN} Range 0 to (V)	V_{OUT} Range (V) to (V)	Bandwidth (kHz)	Slew Rate (V/ms)	Quiescent[3] Current (μA)	I_{OUT} Range (mA)	Offset Voltage (μV)	Bias Current (nA)
OP-90/290/490	1/2/4	1.6–36	$+V_S - 1$	0.6, 4.0[6]	25	10	20	±5	125	4
OP-22	1	3.0–30	$+V_S - 1.5$	0.7, 4.1[6]	200 @ 10 μA[4]	80@10 μA[4]	10–100[4]	±.02 to ±20[4]	400	3[4]
OP-20/220/420	1/2/4	5.0–30	$+V_S - 1.5$	0.7, 4.1[6]	100	50	45	±0.4	300	16
OP-32[5]	1	3.0–30	$+V_S - 1.5$	0.7, 4.1[6]	1000 @ 100 μA[4]	300@100μA[4]	15–450[4]	±.02 to ±20[4]	400	4.5[4]
OP-295/495	2/4	3.0–36	$+V_S - 1$	0, $+V_S$	75	30	150	±3.5	300	8
OP-80	1	5.0–16	$+V_S - 1.5$	0, 3.7	300	400	325	+40, −20	400	0.0006
AD820/822	1/2	3.0–36	$+V_S - 1$	0, $+V_S$	1900	3000	700	±15	300	0.002
OP-292/492	2/4	5.0–36	$+V_S - 1$	0, $+V_S - 1.5$	4000	300	1000	±8	500	350
OP-183/283	1/2	3.0–30	$+V_S - 1.1$	0, $+V_S - 1.1$	5000	10000	1200	±20	300	400
OP-113/213/413	1/2/4	4.0–36	$+V_S - 1$	0, $+V_S - 1$	3500	1000	1400	±30	100	500
SSM-2135	2	4.0–36	$+V_S - 1$	0, $+V_S - 1$	3500	1000	1400	±30	200	300

NOTES
[1]Number of amplifiers on chip: 1—single amplifier, 2—dual, 4—quad.
[2]Total supply voltage span, single or dual.
[3]Per amplifier, using +5-volt supply.
[4]Varies with I_{SET}.
[5]$A_{V(min)} = 10$.
[6]V_{OUT} range can be extended to include 0 volts, using pulldown resistor.

With the exception of parts specified with output swing of 0-to-$+V_S$ (or "rail-to-rail"), most op amps swing to within only 1-to-2 V of the positive rail. So, on supplies of 5 V or less, output swing is greatly reduced in relation to the supply. Even if the input noise floor were to remain constant (which it seldom does), signal-to-noise (SNR) and dynamic range suffer. The sidebar, "Single-Supply Amplifier Output Stages," covers some key factors in single-supply output stage design, and helps differentiate the devices of Table 1 architecturally.

Quiescent Current Drain

Aside from basic cost factors, another fundamental reason for single-supply designs is to conserve power, since they are quite often used in battery-operated equipment. So not only are they designed to perform at very low voltage, but they must also have low quiescent current per channel (I_Q). Unfortunately, low-current designs require basic tradeoffs; in general, sacrifices involve bandwidth, slew rate, and input noise voltage.

Standby current drain (no signal) per amplifier can often be used to qualify a device for critical system power conditions. In the absence of a standard industry definition, we call devices with I_Q of $\leq$1 mA/channel low power, and those with I_Q of $\leq$100 μA/channel micropower. Many of the devices shown in Table 1 meet one or more of these criteria.

Noise Tradeoffs

Bandwidth versus noise is a highly likely tradeoff, as demonstrated by the following examples: the OP-295/OP-495 has input voltage noise of 51 nV/$\sqrt{\text{Hz}}$ at 150 μA/channel, the AD820/AD822 has 12.5 nV/$\sqrt{\text{Hz}}$ at 700 μA/channel, and the OP-113/213/413 family has noise of 4.7 nV/$\sqrt{\text{Hz}}$ at 1.45 mA/channel. Lower noise can be attained at the price of increased current.

Reduced Bandwidth

In a low-power design environment, engineers are forced to face not just generally slower speed in the op amps, but also higher circuit impedances, which themselves can set bandwidth restrictions.

Again, tradeoffs exist. For example the bipolar-input OP-295 has an attractively low current drain of 150 μA/channel, but the bandwidth is 75 kHz with SR of 0.03 V/μs. Where more speed is needed, a FET-input AD820 could be considered, with a 1.9-MHz bandwidth and 3-V/μs SR, at the cost of increased current, 700 μA/channel. Both of these dual devices have rail-to-rail output stages. The OP-183/283 achieve 5 MHz and 10 V/μs, but with current of 1.2 mA/channel.

"Where Is Ground?"

This issue can become quite important in single-supply op amp ac-coupled circuits, since a circuit designer can arbitrarily choose any value for this "false" or pseudo-ground return level. The best choice depends on the application, but a flexible choice of amplifier circuits—and devices that can be used in them, helps make signal referencing easier, particularly in cases where substantial dynamic (i.e., ac) current is present.

Possible choices here range from a simple ac-bypassed resistive divider to fully buffered op amp follower stages that provide the lowest wideband dynamic impedance. A well bypassed noise-free divider is suitable for high-impedance loads, where the dynamic current is low. When dynamic currents are higher, the divider can be buffered with a follower-connected op amp.

AMPLIFIER OUTPUT STAGES

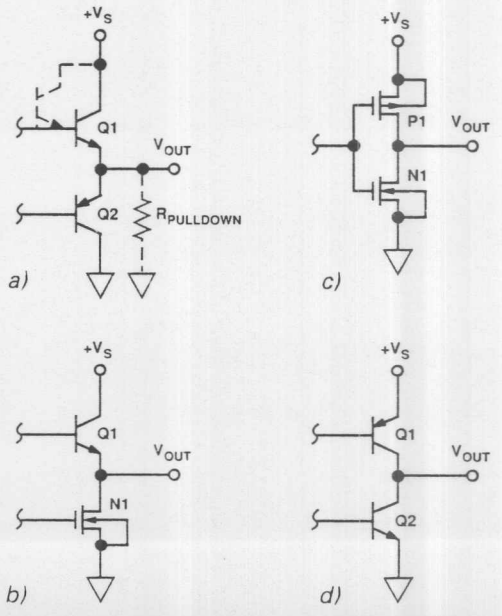
While output swing can be very important in single-supply applications, not all single-supply amplifier outputs are designed to swing all the way to the negative rail (ground). Some may swing to within a diode drop (≈ 0.6 V), others to within a few tens of mV. Only a few swing to within 1 mV of the negative rail—and a precious few swing nearly to *both* supply rails.

To understand which device types work best in applications for which output swing is critical, a designer needs to know about the design of the output stage. These vary widely in detail, so knowledge of their architecture can be critical to an informed selection. The figure illustrates a sampling of some output-stage topologies used in ADI single-supply amplifiers.

The complementary emitter-follower stage of (a), employing bipolar transistors (an NPN transistor for Q1 and a PNP for Q2), can swing to within a diode drop of each rail, at best. It cannot pull right to ground without outside help, such as by adding $R_{PULLDOWN}$, as noted within Table 1 (Note 6). This optional external resistor (which can also include the op-amp's gain-set resistors) bypasses the lower PNP, with its saturation limitation. This technique allows output linearity to ground only when sourcing current; and it can also raise overall dissipation, which may be excessive for sustained high-level outputs. Amplifiers with this type of output have their uses, but should be carefully applied to minimize tradeoffs in single-supply applications. This stage is used in the OP-90/290/490 families, among others.

The output stage of (b) uses a bipolar emitter follower and NMOS common-source. Though inherently asymmetric in terms of voltage swing, it uses the NMOS pulldown to achieve very low saturation voltage to ground. However, saturation voltage to the positive rail is ≥1 V. This stage is used in the OP-113/213/413 families, as well as in the AMP-04 single-supply instrumentation amplifier.

The CMOS stage of (c) is fully complementary and offers a resistive connection to the supply rails for both high and low output, viz., a swing of 0 to $+V_S$, or "rail to rail." With appropriate low-R_{ON} devices for P1/N1, the saturation drop to



either rail can be ≤1 mV at low currents. Because this stage is inherently Class AB, the amplifier design must carefully control the static currents in P1-N1 to maintain low quiescent current. For output currents of a few milliamperes, this type of output stage is effective and quite versatile due to its wide swing. This stage is used in the OP-295/495 families and others.

The complementary-bipolar common-emitter stage of (d) is another rail-rail output stage. Saturation drops range from a few millivolts to a couple of hundred mV, over current ranges of up to about 20 mA. Like the CMOS rail-to-rail output stage, this bipolar counterpart is both effective and versatile, but the design of the amplifier is more critical to avoid tradeoffs in power. This stage is used in the AD820/822 families.

If a reasonably accurate "pseudo-ground" voltage is required, a voltage-reference IC that can source or sink current is desirable, for example, the AD780 or REF-43 (Figure 1). Operating from a 5-V supply, this circuit handles load currents into/from the 2.5-V source with a low ac impedance, aided by the low ESR bypass caps (either tantalum or aluminum electrolytics). The REF-43 provides a 2.5-V output, as does the AD780, with the same pinout. With pin 8 grounded, the lower-noise AD780 can also be used for a 3-V output; and output transient response can be optimized with optional bypass capacitor, C3.

Other low-voltage references worth considering are standard Zener-like two-terminal types, such as the popular AD589, at 1.235 V, operable over current ranges from 50 μA to 5 mA. It can be stacked for higher levels in 1.235-V chunks or scaled up by amplification (see below). With two AD589s stacked in a 3-volt application, a 1.235-volt pseudo-ground is inherent.

Power-Supply Conditioning and Noise

Power-supply noise can defeat even the best paper designs if not properly planned for and dealt with. Low-power analog ICs, which tend to have poor supply rejection, are susceptible to the problem. Commonly used 5-V supplies for computer and digital logic circuitry are especially bad for noise in analog circuitry. Because of both the fast edges inherent in digital circuitry and the prevalent use of switching-type supplies, simple filtering may not be adequate to allow their use with precision analog stages. While use of a supply common to digital circuits may save space and money, its disadvantages should be taken into account where noise is critical.

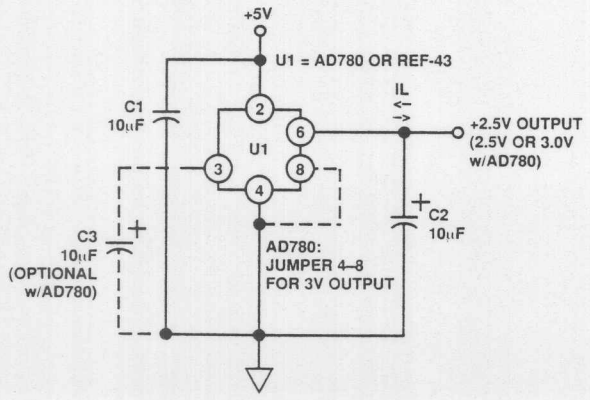


Figure 1. Pseudo-ground at 2.5 or 3.0 V using a reference capable of sourcing and sinking current.

Digital supply feeds taken from the middle of a logic layout contain huge amounts of high frequency noise—100 mV and more. And switching-type logic supplies inherently have large output spikes. It is much better to use a separate, low noise linear-mode supply for sensitive analog circuits where possible.

If a 5-V logic supply must be used, isolation and circuit partitioning can help greatly, as can optimized decoupling and filtering. Make sure that power for analog circuitry is wired directly to the supply terminals, not from downstream logic stages. This avoids both static and dynamic voltage drops due to logic currents and their rapid fluctuations.

Bypass capacitors are usually not by themselves adequate for filtering switch-mode glitches, so additional steps should be taken. For example, one can isolate logic noise with a balanced in-line LC filter[1, 2]. This filter uses a high-capacitance composite output capacitor and two high-frequency inductors—one in each line—made from a "three-turn" [actually two complete turns] wrapped toroidal ferrite bead. The capacitors, made up of a paralleled 100-μF electrolytic, 10-to-22-μF tantalum, and 0.1-μF ceramic, can be low-ESR switching types for best performance, but this is not absolutely essential. Such filters can suppress logic glitch noise by 40 dB and more.

Watch Out for Circuit-Dependent Swing Limitations

Even if a device has wide output-swing capability, the application configuration can have swing limitations. For example, consider the popular two-op-amp instrumentation amplifier (in-amp) shown in Figure 2; normally a dual-supply design, it is adapted here for single-supply use with selectable gains of 10× or 100×. At first glance, one might expect that this 100× instrumentation amp should easily amplify small positive voltages, e.g., a +10-mV differential input [$V_{IN}(-) = 0$, $V_{IN}(+) = 10$ mV] to produce +1 V at V_{OUT}. However, even with near-perfect characteristics for amplifiers A and B, closer examination shows a potential difficulty. Note that to satisfy loop requirements and produce 1 V at V_{OUT}, V_{OA} must be 0 V while sinking current, a factor which demands ideal saturation characteristics of U1A. Practically speaking, this in-amp configuration needs excellent output characteristics in both amplifiers for best linearity.

The point is that, even though an op amp may be well-designed for single-supply operation, its performance can still be constrained by the chosen configuration. It's also worth noting that if a 5-resistance in-amp topology is used to obtain single-resistor gain-setting (4 fixed resistances plus a variable gain-setting

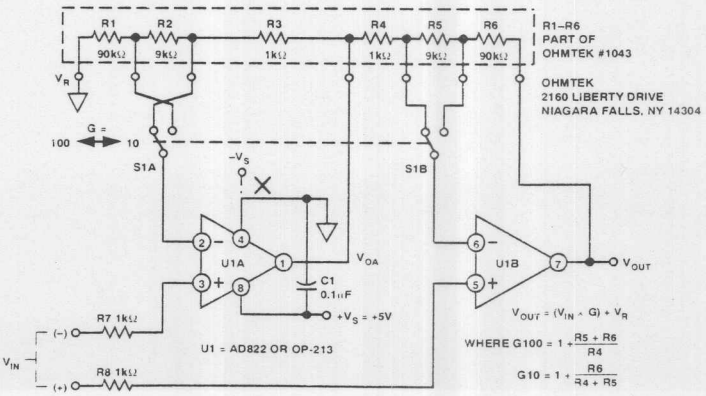


Figure 2. Two-op-amp programmable-gain instrumentation amplifier for single-supply applications.

resistor connected between the summing points), the ideal voltage output demanded of amplifier A can be negative! Thus, although rail-to-rail output-stage op amps help improve CM handling (see sidebar), topology is also important to performance.

In spite of these inherent limitations, the topology of Figure 2 is still very useful when carefully applied. For gain of 100, the circuit provides subtraction with gain (and common-mode rejection) when the two ratios, $(R_1 + R_2)/R_3$ and $(R_5 + R_6)/R_4$, are equal. The 100× gain (G = 100) is equal to $1 + (R_5 + R_6)/R_4$. In the switch's gain of-10-position, the gain is $1 + R_6/(R_5 + R_4)$. For either gain, the resistor ratios on both sides must be equal for good CMR.

This approach has advantages and disadvantages in practical implementation. It is not as simple in concept to gain-program as the 5-resistor topology (which simply adds an R_G resistor between the summing points of a 4-resistor ratio-matched network). However, it's worth noting that, in the topology of Figure 2, 10-to-100 Ω of series switch resistance has negligible effect on gain accuracy, while it would have significant impact when switching R_G in the five-resistance topology.

Keys to performance of this circuit are the resistor network and the amplifier. For best performance with premium amplifiers, the network should have a ratio-match specification of 0.1% minimum, and 0.01% as a goal. For ideal amplifiers, the output CM error due to 0.01% match resistors will be of the order of −100 dB for a gain of 10, or −120 dB for a gain of 100. The suggested network is available with ratio-matching to 0.01%.

The circuit can be easily gain-switched with jumpers, or CMOS switches, e.g., a 3.3- and 5-volt-specified DPDT ADG513 quad switch, used as shown. Operating on single supplies, the CM limitations of the configuration must be observed, as noted. V_{OUT} will be referred to the potential applied to the network's V_R pin (but watch out for potential difficulties due to inverted V_R on the intermediate output, V_{OA}; $V_{IN}(-)$ must be more positive than V_R). With dual supplies ($-V_S$ connected as noted), these caveats are eased.

Suggested amplifiers for U1 are either the AD822 or an OP-213, depending on source resistances at V_{IN}. The AD822 is available with offset as low as 0.4 mV and typical drift of 2 μV/°C; it is well suited to high impedances calling for very low bias currents, a circumstance found in bio-medical applications, high-Z bridges, etc. The OP-213, with its offset of 150 μV and typical drift of 0.2 μV/°C, will be better suited to those uses requiring lowest noise and/or drift—especially at high gains—such as load cells.

Look for Devices Designed for Single-Supply Use

The discussions above should make one general point clear: for designs requiring single supplies, it is usually most fruitful to employ amplifiers expressly designed for the job. Among the performance specs that will be enhanced are supply power and operating ranges, dynamic range, input/output ranges, and increased overall linearity. In addition to the sampling of newer op amp types (Table 1), there are other IC devices designed for single-supply/low power operation.

We've briefly discussed references here, mentioned the ADG511/12/13 switch series, and considered the design of high-input-impedance instrumentation amplifiers for single supplies. Although endowed with somewhat lower input impedances, the AMP-04 single-supply in-amp (*Analog Dialogue* 27-1) and the AD626 low-cost single-supply (+2.4 to +10-V) differential amplifier, with fixed gains of 10 and 100 (*A-D* 26-1), are worthy of mention. Tables 2 and 3 illustrate typical characteristics of general-purpose Analog Devices single-supply ADCs and DACs that are specified to operate on +5-V single supplies. While space does not permit detailed discussion of their performance, these data can serve as an introduction to what is available for systems employing A/D and D/A conversion.

Table 2. A/D Converter Chips Compatible with Single-Supply Systems

Device	Resolution (Bits)	Multiplex Capability (Channels)	Supply Voltage (V)	Input Range 0 to (V) or (±V)	Output Format Ser/Par	Reference Ext/Int (V)	Architecture Type	Conversion Speed ksps
ON-CHIP SAMPLING								
AD7575	8	1	5	2.46	Parallel[4]	Ext 1.23	Successive apx	200
AD7820	8	1	5	5	Parallel[4]	Ext	Half-flash	500
AD7821	8	1	5[1]	5, ±5	Parallel[4]	Ext	Half-flash	1000
AD7824/28	8	4/8	5	5	Parallel[4]	Ext	Half-flash	400
AD7579/80	10	1	5	2.5, 5, ±2.5	Parallel[4]	Ext 2.5	Successive apx	50
AD7776	10	1	5[1]	2	Parallel	Ext/Int	Successive apx	400
AD7777	10	4	5[1]	2	Parallel	Ext/Int	Successive apx	400
AD7778	10	8	5[1]	2	Parallel	Ext/Int	Successive apx	400
AD7880	12	1	5[5]	5, 10, ±5	Parallel	Ext	Successive apx	66
AD7883	12	1	3[5]	3, 6, ±3	Parallel	Ext	Successive apx	50
AD7890-x[2]	12	8	5	2.5[2]	Serial	Ext/Int	Successive apx	100
AD7893-x[3]	12	1	5	2.5[3]	Serial	Ext 2.5	Successive apx	117
AD7710/11/12/13	24	1-3[6]	5[1]	0.02, 2.5	Serial	Int	Charge-bal[7]	Filter-dep.
OFF-CHIP SAMPLING								
AD670	8	1	5	0.255, 2.55	Parallel[4]	Int	Successive apx	10 μs
AD875	10	1	5[5]	2 V p-p	Parallel[4]	Ext 2.0	Pipelined flash	15000
AD776	16	1	5	4	Serial	Ext/Int	Sigma-delta	100

NOTES
[1]Operates with wider (or dual) supply range also.
[2]Input range is 0 to 2.5 V for AD7890-2, 0 to 4.096 V for AD7890-4, ±10 V for AD7890-10.
[3]Input range is 0 to 2.5 V for AD7893-2, 0 to 5 V for AD7893-5, ±10 V for AD7893-10.
[4]Three-state output interface.
[5]Power-down function available.
[6]On-chip programmable-gain amplifier, G = 1 to 128.
[7]On-chip microcontroller, auto-zero and auto-cal functions.

SINGLE-SUPPLY CIRCUIT APPLICATIONS

Some selected applications illustrate the general design concepts discussed above.

References for Low Power Systems

There are a variety of considerations when stable, accurate dc voltage references are made to work from 5 V (and lower) supplies. These include: quiescent power consumption and overall power efficiency, the ability to operate down to 3 V, low input/output (dropout) capability, and minimizing noise output. Because supplies less than 5 V can't support devices such as buried Zener diodes, low voltage references must necessarily be bandgap types. Figure 3 and 4 show reference circuits that can work at >3 V.

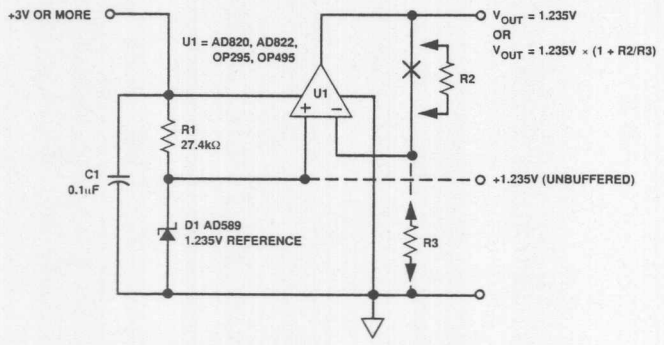


Figure 3. Buffered reference for 1.23 V or more, using a supply voltage ≥3 V.

It is difficult to get a reference to work well down to 3 V, a condition that dictates use of a lower-voltage reference diode. A solution is a two-terminal (hence "diode") 1.235-V reference based on a bandgap circuit, and appropriate low-power support circuitry, as shown in Figure 3.

Table 3. D/A converter chips compatible with single-supply systems

Device	Resolution (Bits)	DACs (Channels)	Supply Voltage (V)	Output Range 0 to (V) or (V±V)	Input Format[5] Ser/Par	Reference Ext/Int (V)
AD557	8	1	5	2.56	Parallel	Internal
AD558	8	1	5 to 15	2.56, 10	Parallel	Internal
PM-7528	8	2	5[1]	1.23[2]	Parallel	External 1.23
DAC-8408	8	4	5	1.23	Parallel[3]	External 1.23
PM-7226A	8	4	5[1]	1.23	Parallel	External 1.23
AD7228A	8	8	5[1]	1.23	Parallel	External 1.23
DAC-8841	8	8	5	3	Serial[4]	External 1.5
ADV7128	10	1	5	0-17.61 mA[6]	Parallel	External 1.23
DAC-8512	12	1	5[1]	4.095	Serial[4]	Internal
DAC-8562	12	1	5[1]	4.095	Parallel	Internal
DAC-8221	12	2	5[1]	1.23[2]	Parallel	External 1.23
DAC-8222	12	2	5[1]	1.23[2]	Parallel	External 1.23
DAC-8248	12	2	5[1]	1.23[2]	Parallel	External 1.23
DAC-8412/13	12	4	5[1]	2.5	Parallel[3]	External 2.5
DAC-8420	12	4	5[1]	2.5	Serial	External 2.5
AD1866	16	2	5	2.5±1	Serial	Internal
AD1868	18	2	5	2.5±1	Serial	Internal

NOTES
[1]Operates with wider supply range also.
[2]Unbuffered analog output (≈11 kΩ).
[3]Read/write parallel interface.
[4]Three-wire serial interface.
[5]Internally latched.
[6]Video level of 0.6 V into 37.5 Ω (75 Ω double-terminated).

The low-current diode used for D1 is the 1.235 V AD589. Resistance R_1 sets the current, chosen for the device's minimum specified current, 50 μA (5-mA max), at a minimum supply of 2.7 V. At this low value of current, loading on the unbuffered diode must also be minimized, but generally static loads of a few μA are all right (if accounted for). The dynamic impedance of the diode decreases to about 1 ohm with 500 μA.

Amplifier U1 buffers and scales the 1.235-V reference, so that higher source or sink load currents can be handled. The cost is 150 μA of quiescent current through U1, using one channel of an OP-295, or 700 μA using an AD820. Without gain scaling resistances, R_2-R_3, the output is simply 1.235 V; with these resistors, the output can be set anywhere between the supply rails, due to the specified device's rail-to-rail range. This buffered reference is inherently "low dropout"—furnishing a +4.5-V reference output on a +5-V supply, for example.

Noise output will be dominated by the diode's ≈ 100 to 200 nV/$\sqrt{\text{Hz}}$, but this can be filtered (as the next circuit shows); with an AD820 one achieves lowest overall noise and substantial drive current (15 mA).

Amplifier standby current can be optionally reduced to 20 μA if an OP-90 is used, and all devices mentioned operate from supplies as low as 3 V. Output voltage drift, primarily a function of the diode grade, can be as low as 10 ppm/°C.

Low-Dropout Regulators

With a boost transistor added within a low-dropout reference circuit, output currents >100 mA are possible, while still retaining low standby current and low dropout voltage.

Figure 4 shows a low-dropout regulator with 800 μA of standby current, suitable for a variety of voltages and output currents up to 100 mA. It achieves a 100-mA current using a controlled-gain pass transistor, Q1, an MJE170 type. Output current control is provided by limiting base drive to Q1 by a series resistance, R_3. This limits the base current to about 2 mA, so that with maximum HFE of Q1, no more than 500 mA is allowed to flow, limiting short-circuit dissipation to safe levels (if a heat-sink and fuse are employed).

Output voltage level is chosen simply by programming R_1 according to the table. Dropout with a 100-mA load is about 200 mV; thus a 5-V output is maintained for inputs above 5.2 V (see table). Output voltages down to 3 V or less are possible.

The circuit responds well to stepped loads; transient error is only a few mV, p-p, for a 30-100-mA load change. This is achieved

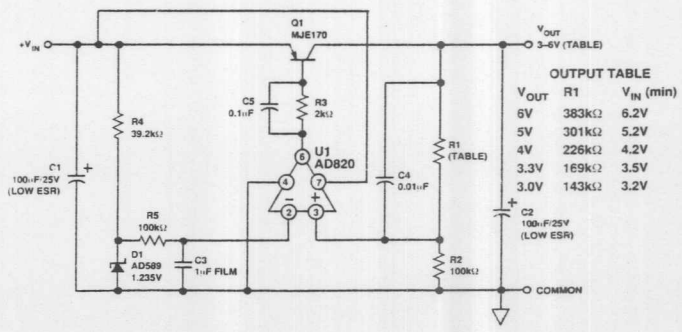


Figure 4. Low-dropout, low-noise, low-voltage regulator capable of 100-mA output.

partially through the use of low ESR switching type capacitors (C_1-C_2); the circuit also works with smaller value conventional electrolytics (but with greater errors).

Low output noise is attained in this circuit with the reference filter, R_5-C_3. An OP-295 can be used as the amplifier; it allows lower overall standby current ($\approx$ 200 μA), but has greater transient errors due to reduced bandwidth.

4-20 mA Loop Circuits

Amplifier devices with outputs that swing close to the negative rail enhance and/or simplify 4-20-mA loop transmitter designs, as exemplified in Figure 5. In this loop-powered strain-gage sensor application, a 50-mV full-scale (FS) bridge output is amplified and calibrated for a 4-20-mA transmitter output. Power is furnished by the remote loop supply of 12 to 36 V.

U1, an AMP-04 single-supply in-amp, amplifies the bridge signal with a gain of about 40 V/V; [G = 100,000/R_G]. The AMP-04's output range includes the negative rail, so a 0 to 50-mV bridge signal is amplified to 0 to 2.01 V, referred to the common bus (U1, pin 5). With all the devices' negative supply pins referred to this bus, the bulk of the loop quiescent current flows through R_6, the external loop, and termination, R_{LOAD}.

U2 acts as a summing V-to-I converter, which produces an output span of 0 to 16 mA, proportional to the bridge output signal. In addition, since the total quiescent current of the circuit adds up to something less than 4 mA, U2 produces an incremental reference offset to bring the minimum loop current up to 4 mA. The signal and reference voltages are converted to currents, which are summed and flow through R_5. The output of operational amplifier, U2, drives pass transistor, Q1, to produce a current flowing through R_6 such that its voltage drop must equal that in R_5, in order to maintain the summing point, pin 3 of U2, at a null.

With zero bridge output, U1's output will be at the negative rail. No current flows into the summing point of U2 via R_1-R_2, since the summing point is at this same potential. For this zero-signal condition, the loop is calibrated via R_3 (NULL, or reference) to produce a 4-mA output current, or 0.4 V across a 100-Ω R_{LOAD}. With zero current through SPAN adjustment, R_1, the 4 mA can be set independently. The NULL-SPAN trims are inherently non-interactive because of the null at the summing point of U2.

R_3 and R_4, connected between the output of 5-volt-reference U3 and the summing point's virtual ground, produce the constant incremental reference current, which is scaled by the loop current-gain resistors, R_5 and R_6. This current, I_{NULL}, is:

$$I_{NULL} \approx \left[\frac{5\ V}{R_3 + R_4}\right]\left[1 + \frac{R_5}{R_6}\right]$$

where 5 V is the output of reference U3, which is driven by the remote loop supply. R_3 is adjusted to set I_{NULL} for 4-mA loop current.

The bridge output is amplified (to 2.01-V for 50-mV bridge output) by U1, and converted to signal current to the U2 summing point by R_1 and R_2. There it is summed with the incremental reference current, and amplified by R_5 and R_6. Its contribution, I_{SPAN}, is:

$$I_{SPAN} \approx \left[\frac{G\ V_{BRIDGE}}{R_1 + R_2}\right]\left[1 + \frac{R_5}{R_6}\right]$$

where V_{BRIDGE} is the output of the bridge, and G the AMP-04's gain. Full-scale current output is trimmed by adjusting R_1 (SPAN), with a 50-mV FS bridge output, for 20-mA output current (4-mA quiescent-current-plus-I_{NULL} plus 16-mA I_{SPAN}), or 2 V across R_{LOAD}.

In this circuit the three active devices and the 3500-Ω bridge consume 3.75 mA maximum, less than the system's 4-mA reference level, so some NULL current is always needed. C_1 provides 7-Hz low-pass filtering, to limit noise, while C_2 stabilizes the U2 output loop. The 0-to-16-mA I_{SPAN} portion of the loop output, plus the NULL current, is passed by Q1 (TO-220 package).

5-V Single-Supply D/A Converters

At present, most of the available DACs (D/A converters) require dual power supplies. For those that don't, supplies of 12-to-15 V are usually required. At the moment, this factor limits DAC choices for use with single +5-V supply system power.

CMOS R-2R ladder DACs are a natural choice for low-power operation; and many of these units are designed to work on 5 V supplies. However, if used in the standard multiplying mode they also require a negative supply for the inverting output amplifier, and they require a negative reference for positive output (or vice versa). In order to make such a DAC operate on a single polarity, it can be turned around and operated in what is known as its inverted, or voltage output mode. Most CMOS R-2R DACs can operate in this fashion, even if not specified to do so[3, 4] (see Table 3, again).

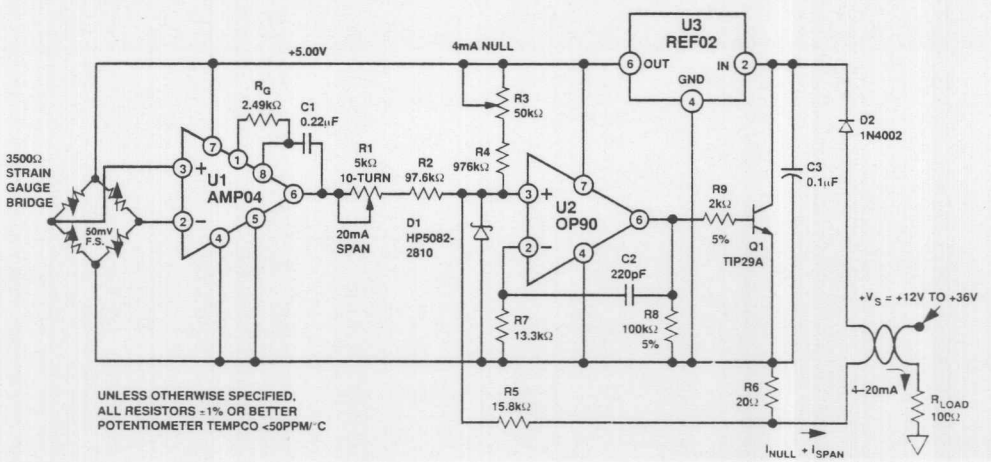


Figure 5. Precision bridge-output-to-4-20-mA-loop transmitter with non-interactive trims deriving all excitation functions from loop supply.

Using a 12 bit DAC-8043 in this mode with the pinout shown in Figure 6, the ladder input labeled V_{REF} becomes the voltage output node (pin 1), and the normally I_{OUT} node becomes the reference input (pin 3). This voltage-mode CMOS DAC circuit, using two 8-pin ICs and interfacing serially, works on a single 5 V supply; it is scaled for 0-to-4.095-V output range (or 1 mV/LSB).

The circuit is clean and straightforward, but some practical points are worth noting to obtain best results. With a 5-volt supply, the internal NMOS switches have only [5 V − V_{REF}] as enhancement voltage, or 3.765 V with a 1.235-V reference. This is about as high a reference voltage as one should apply to the DAC operating in this fashion. If higher V_{REF} values are used, the MOSFET gate drive can become starved, resulting in higher On resistance and nonlinear output voltage.

This circuit uses an DAC-8043, a 12-bit multiplying DAC, so the output voltage will be [D/4096]*V_{REF}, where "D" is the numerical value of a 12 bit digital word—ranging from 0-4095. With V_{REF} = 1.235 V, the unbuffered output at pin 1 of U1 is [4095/4096]*1.235 V at all-1s, or [full-scale − 1 LSB].

The output amplifier, U2, amplifies the voltage at the DAC output by the gain value, G, to meet the needs at its destination. The resistance values are chosen here to provide a scale factor of 1 mV/LSB with an appropriate adjustment of R_4. The gain required of U2 for this weighing is about 3.3, and is made variable to trim out tolerances in both the reference voltage and gain resistors. Also, to balance out voltage offsets due to bias current (for amplifiers where this is a consideration), the values chosen help to make the equivalent resistance of the gain divider equal to the DAC output resistance, ≈ 11 kΩ.

For a linear V_{OUT} range of 0 to 4.095 V, the amplifier must be capable of rail-to-rail output, for example, the OP-295 or the AD820 (AD822). DC accuracy, speed, and power are strongly affected by the choice of U2, and some tradeoffs may be necessary for the best overall choice. Relatively slow response and best overall DC accuracy is possible with the OP-295—or faster response with good, but somewhat reduced, accuracy using the AD820. The OP-295 has a max V_{OS} of 300 μV, so worst-case output offset is about 1 mV; with the AD820B this increases by a factor of 1.3 (and can be optionally nulled).

Both amplifiers can source a 4.095-V output, using a 4.75-V supply, with the AD820 capable of 10 mA, the OP-295, 5 mA. The rail-to-rail output stages of both allow linear swings close to ground. For the OP-295, the CMOS output stage allows linear outputs to within ≤1 mV of ground, while the bipolar output of the AD820 pulls down to about +5 mV.

Settling time using the OP-295 is below 150 μs, but the AD820 can improve it to about 2.5 μs, due to the higher slew rate. The tradeoff here is power; one channel of an OP-295 with the DAC consumes about 660 μA, while the faster AD820 uses ≈ 1.2 mA.

Complete, single IC buffered 12 bit single-supply DACs are also available, and the function just described can be realized in both serial and parallel input formats with the DAC-8512 and DAC-8562, respectively, as noted in Table 3.

Precision Temperature Sensing

Many methods of sensing temperature are available, but very high precision on single power supplies remains a challenge. Figure 7 shows how a precision platinum resistance-temperature-device (RTD) sensor circuit can be implemented on 5 V. The RTD bridge is driven with a regulated 200-μA current, I_{BRIDGE}, minimizing self-heating. Overall current drain is 1.3 mA, and the circuit works from supplies of 5 V for a 0-400°C output, or as little as 4.5 V for 0-350°C.

The 200-μA current is sensed by R_{SENSE}, and the voltage it develops across the 1-kΩ resistor is compared to a 0.2-V reference appearing across R_5 in the U1-A control amplifier—an OP-295, which allows input voltages of 0.2 V. The rail-to-rail output provides ample bridge-drive headroom. At the bridge output the common-mode voltage is 0.21 V, a difficult-to-handle level for conventional 5-V in-amps, IC or discrete. In this circuit the output is amplified by U3, an AMP-04.

This device has an input CM range of 0-3.5 V and an output range of 0 to 4.2 V, operating on 5 V. The AMP-04 gain with the value of R_{GAIN} shown here is nominally 245, and this gain times the bridge output voltage of 38 μV/°C yields a V_{OUT} sensitivity of 10 mV/°C. C_1 provides a low-pass filter function in conjunction with a 100-kΩ resistor inside the AMP-04, with 3.4-Hz cutoff.

Several factors concerning the surrounding circuit are important for best performance. All critical resistors(*) should be 0.5%, ±25 ppm/°C types, or about 100 times better than the RTD's temperature coefficient (TC) of 3850 ppm/°C. R_1-R_2, in particular, should be same-manufacturer/same-batch units, with R_4 by the same manufacturer (all of which helps minimize differential TCs. Gain resistance, R_8, should have a TC low with respect to

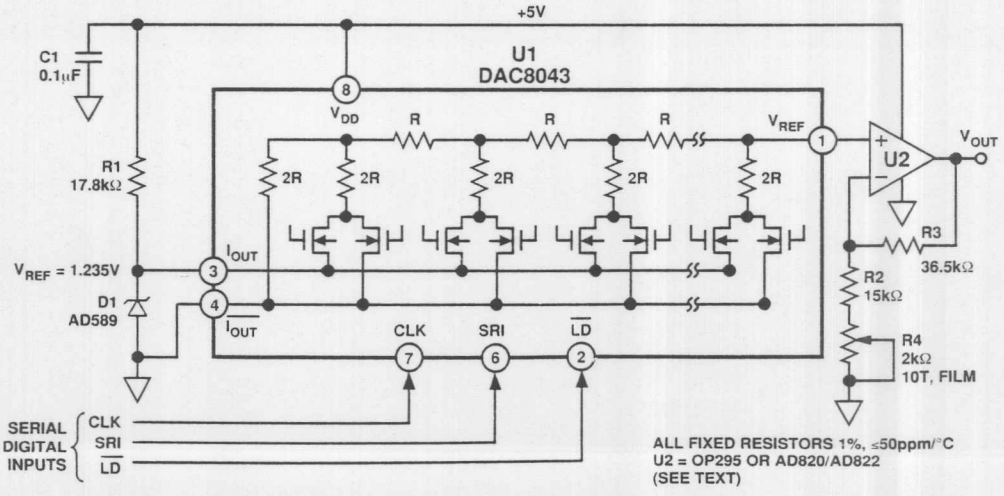


Figure 6. 12-bit DAC with rail-to-rail output buffer for single +5-V supply.

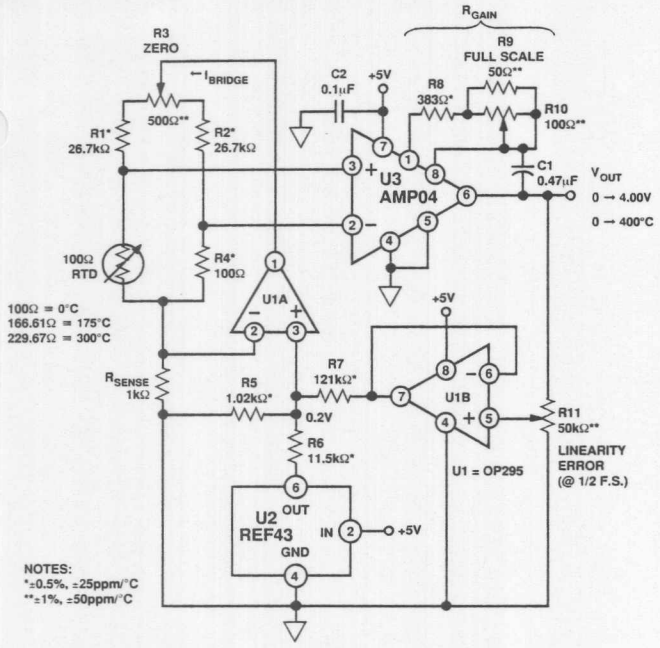


Figure 7. Precision single-supply RTD bridge and amplifier with feedback linearization.

the AMP-04's TC (50 ppm/°C). Less-critical resistors (**) with smaller percentage-error contributions can be more loosely controlled. All trimmers should be multiple-turn film types.

The bridge/amplifier combination has a small amount of non-linearity, typically ≤0.5%. In comparison, the RTD has a much larger non-linearity, as much as 6°C over a 400°C span, or 1.5%. Fortunately, this non-linearity can be corrected with controlled positive feedback, increasing bridge drive with increasing output. A fraction of V_{OUT} is picked off by R_{11}, buffered by U1-B, and summed with the reference voltage via R_7. With correct adjustment, this cancels the RTD non-linearity.

Calibration is a relatively simple 3-step process. First, care must be taken in setting for 0°C, since the lack of a negative supply prevents this end point from attaining 0 V. One technique (step 1) is to substitute a resistance of exactly 100 Ω for the RTD (or place the actual RTD in an ice bath solution), and adjust R_3 (ZERO) until V_{OUT} begins to swing positive. Then, trim R_3 in the reverse direction until V_{OUT} just stops changing, which should be at 0 V.

For the FULL-SCALE trim (step 2), preset R_{11} to a midpoint and substitute a 274.04-Ω resistor for the RTD. Then trim R_9 for 4.000 V at V_{OUT} (400°C). For LINEARITY (step 3), substitute a 175.84-Ω resistor for the RTD, and trim R_{11} for 2.000 V at V_{OUT}. Steps 2 and 3 should be repeated for best accuracy, as they interact. When fully trimmed, the output errors of the circuit are within ±0.5°C over the 0 to 400°C range

Single-Ended High-Impedance Microphone Preamp

The microphone preamplifier is a basic audio low-level circuit. While it can assume a variety of forms, designs for low-voltage, single-supply systems can be particularly challenging, because there are few devices with really low noise on 5-V power. The choice gets easier if the total supply voltage is ≥10 V, or if a higher-voltage dual supply can be used.

Figure 8 shows a simple non-inverting stage with a single-ended input, a useful approach with high-impedance microphones—higher-Z dynamic types and crystal or ceramic piezoelectrics. The circuit, with a gain range of 20-40 dB, can be readily optimized for microphones with impedances ≥600 Ω. The op amp used for U1 affects performance in general and suitability for single-supply operation. U1 should preferably have low input noise with ≥500-Ω sources. The most suitable types are the AD820, and the dual SSM-2135 and AD822.

Gain-determining resistors, R_1 and R_2, are scaled for parallel resistance less than the expected source impedance, to minimize their noise contribution at high gain. Gain is adjusted with R_2, while capacitors C_1, C_2, and C_3 decouple dc levels. The amplifier biasing and resistors must not introduce noise, even indirectly[5]; thus, resistors with dc across them (R_1, R_3, R_7, and R_8), and the gain resistors, should have low excess noise—metal films are preferred—or be bypassed (R_7, R_8). R_7-R_8 bias the U1 output to 2.2 V (in this case) for maximum symmetrical output swing.

While the SSM-2135 is optimum when operating from low-impedance sources, the FET-input AD820 (or AD822) is preferable with high-impedance crystal or ceramic mikes. For such sources, R_3 and R_4 should be 1 MΩ or more, with C_1 a 0.1-μF film capacitor. The input cable to the microphone must be short and shielded. With symmetric dual supplies, R_3 is grounded and $-V_S$ is applied to U1; Xs mark the spots.

Bandwidth at maximum gain is about 30 kHz with the SSM-2135, 20 kHz with AD820. With a shorted input, the SSM-2135 measures an output noise of about 110 μV rms at a gain of 100, and 0.022% 1-kHz THD+N with 1 V rms into a 2-kΩ load. Similar tests with the AD820 give about 200 μV rms and 0.05% THD+N. All figures improve at lower gains. ◘

REFERENCES

1. W. Kester, ADI Staff, *Amplifier Design Guide* [Analog Devices Amplifier Seminar Notes], 1992. Use book purchase card or phone or fax ADI Literature Center. See also P. Brokaw, "An I.C. Amplifier User's Guide to Making Things Go Right for a Change," Analog Devices Application Note AN-202. Circle 11
2. J. Wong, "Simple Filter Quiets Power Line," *EDN*, June 4, 1992.
3. J. Wynne, "12-Bit Voltage-Output DACs for Single-Supply 5-V & 12-V Systems," 1991. Analog Devices Application Note AN-225. Circle 69
4. D. Sheingold, ed., *Analog-Digital Conversion Handbook*, 3rd edition (1986), pp. 202-203. Englewood Cliffs, NJ: Prentice Hall (also available from Analog Devices. Use book purchase card or phone or fax ADI Literature Center.).
5. C. Motchenbacher, F. Fitchen, *Low-Noise Electronic Design*, New York: Wiley, 1973.

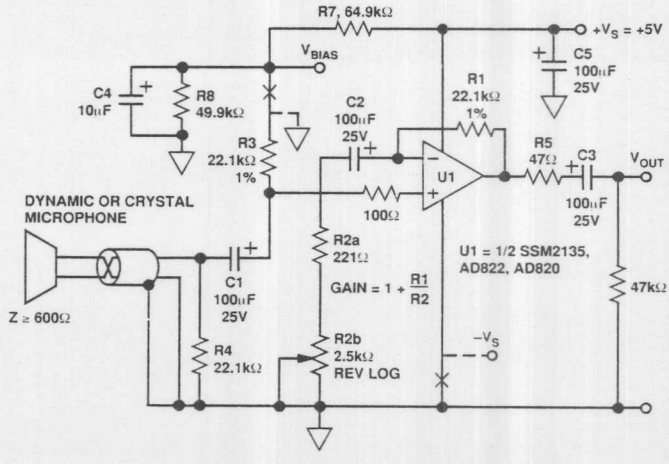


Figure 8. Single-ended, single-supply, high-impedance microphone preamplifier is useful with various microphone types.